Low Power Operation in Fir Filters using Vedic Based Multiplication

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Abstract:
FIR Filter has widespread applications in signal processing such as image processing, biomedical signal processing, high speed communication systems, noise elimination and many more. The speed of FIR filter can be improved with high speed multipliers and with low propagation delay adders. In this paper we will discuss in detail about different reconfigurable FIR filter architectures and propose a modified minimum switching activity booth multiplier . Although all those three FIR filter architectures are reconfigurable but each of them have different complexity based on the way processing elements are implemented. Each of them has its own merits and demerits compared with the other methods. Xilinx 12.1 result shows better time and area reduction for our proposed fir filter implementation

1 INTRODUCTION

FIR Filter has across the board applications in signal processing, for example, picture handling, biomedical signal processing, rapid correspondence frameworks, noise elimination and many more. The speed of FIR filter can be enhanced with fast multipliers and with low engendering postpone adders. In this paper we will talk about in insight about various reconfigurable FIR filter models. Albeit every one of those three FIR channel structures are reconfigurable yet each of them have distinctive unpredictability in view of the way preparing components are actualized. Each of them has its own benefits and faults contrasted and alternate strategies.

Filtering is a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal. Most often, this means removing some frequencies and not others in order to suppress interfering signals and reduce background noise. Filters can be classified in several different groups, depending on what criteria are used for classification. The two major types of digital filters are finite impulse response digital filters (FIR filters) and infinite impulse response digital filters (IIR).

Finite Impulse Response (FIR) filter are of great importance in digital signal processing (DSP) systems since their characteristics in linear phase and feed forward implementation make them very useful for building stable high performance filters. The direct and transposed form FIR filters implementations are mostly use in the context of digital filters. Although both architectures have similar complexity in hardware, the transposed form is generally preferred because of its higher performance and power efficiency. The multiplier block of the digital FIR filter in input stage is very compact structure because of the complexity and performance of the design

Techniques for reducing power consumption have become important due to the growing demand for portable multimedia devices. Since digital signal processing is pervasive in such applications, it is useful to consider how algorithmic approaches may be exploited in constructing lowpower solutions. A significant number of DSP functions involve frequency selective digital filtering in which the goal is to reject one or more frequency bands while keeping the remaining portions of the input spectrum largely unaltered. Examples include lowpass filtering for signal upsampling and downsampling, bandpass filtering for subband coding, and lowpass filtering for frequency-division multiplexing and demultiplexing. The exploration of low-power solutions in these areas is therefore of significant interest. Reconfigurable hardware architectures are emerging as a suitable approach to combine high performance with flexibility and programmability. Recently, with the advent of software defined radio (SDR) technology, finite impulse response (FIR) filter research has been focused on reconfigurable realizations. The fundamental idea of an SDR is to replace most of the analog signal processing in the transceivers with digital signal processing in order to provide the advantage of flexibility through reconfiguration. This will enable different air-interfaces to be implemented on a single generic hardware platform to support multi-standard wireless communications. Wideband receivers in SDR must be realized to meet the stringent specifications of low power consumption and high speed

2 FIR FILTER THEORY

The most common digital filter is the linear time-invariant (LTI) filter. An LTI interacts with its input signal through a process called linear convolution, denoted by y = f x where f is the filter's impulse

response, x is the input signal, and y is the convolved output. The linear convolution process is formally defined by:

$$y[n] = x[n] * f[n] = \sum_{k=0} x[n]f[n-k] = \sum_{k=0} f[k]x[n-k].$$

LTI digital filters are generally classified as being finite impulse response (i.e., FIR), or infinite impulse response (i.e., IIR). As the name implies, an FIR filter consists of a finite number of sample values, reducing the above convolution sum to a finite sum per output sample instant. An FIR with constant coefficients is an LTI digital filter. The output of an FIR of order or length L, to an input timeseries x[n], is given by a finite version of the convolution sum given in (1), namely:

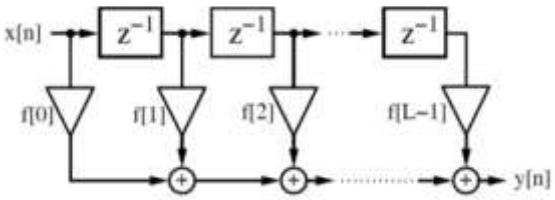
$$y[n]=x[n]*f[n]=\sum_{k=0}^{L-1} f[k]x[n-k],$$

where f[0] • 0 through f[L í 1] • 0 are the filter's L coefficients. They also correspond to the FIR's impulse response. For LTI systems it is sometimes more convenient to express in the z-domain with

where F(z) is the FIR's transfer function defined in the zdomain by

$$F(z)= \sum_{k=0} f[z]z^{-k}$$

The Lth-order LTI FIR filter is graphically interpreted in Fig.1. It can be seen to consist of a collection of a "tapped delay line," adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient, often referred to as a "tap weight" for obvious reasons. Historically, the FIR filter is also known by the name "transversal filter," suggesting its "tapped delay line" structure[7]



3 RELATED WORK

In [1] author proposes , a new design approach to implement an FIR filter using canonical sign digit (CSD) multipliers based on modified decorrelating transformation (MDECOR). The direct CSD approach will introduce serious quantization errors since the distribution of CSD numbers is very non-uniform. The proposed MDECOR transformation provides a systematic solution to reduce the dynamic range effectively. By combining the proposed MDECOR transformation followed by CSD quantization, we can avoid the aforementioned quantization problem. As a result, we do not need to employ additional non-zero bits to compensate for the distortion caused by direct CSD quantization, which helps to save the number of adders in VLSI implementations

In [2] author proposes ,proposed method by considering the filter coefficient and inputs, filter dynamically changes the filter order to achieve dynamic power savings with minor degradation in performance. When the multiplication of input data and filter coefficient is so small the multiplication operation is cancelled and the multiplier is turned off to reduce the power consumption

In [3] author proposes, propose an effective alternative that distributes a pre-defined addition budget to the multiplier-less FIR filters, which takes into account the common sub-expression sharing inside the computations. We successfully integrate a heuristic common sub-expression elimination (CSE) algorithm and the coefficient quantization by successive approximation proposed by Li et al. Besides, we also propose an improved search algorithm for an optimal scale factor to settle the coefficients collectively into the quantization space

In [4] author proposes, presented low power and high-speed realisation of differential-coefficients-based finite impulse response filters. The conventional differential coefficients method (DCM) uses the difference between adjacent coefficients whereas we identify the coefficients that have the least difference between their magnitude values and use these minimal difference values to encode the differential coefficients. Our minimal-difference differential coefficients can be coded using fewer bits, which in turn reduces the number of full additions required for coefficient multiplication. By employing a differential-coefficient partitioning algorithm and a pseudofloating-point representation

In [5] author presents a low power programmable FIR filter based on partitioned multipliers. Architecture chosen for implementation is conventional direct form. Power efficient techniques like unsigned multiplication and reduction of switching activity are used. Paper presents power, area and speed analysis of the proposed design. FIR Filter is fully parameterized, dynamically programmable and technology independent

In [6] author proposed method is based on the masking method and the techniques for rounding and sharpening. The coefficient values of the model and masking filters are represented as integers using the rounding technique. The sharpening technique is applied to improve the overall magnitude

characteristic and to satisfy the given specificationModified Booth Algorithm

Vedic Multiplier

The former practices were recalled from Indian Sanskrit works named as the Vedas,concerning 1911 in addition to 1918 by Sri Bharati Krishna Tirthaji and from (1884-1960) the Atharva Vedas. As indicated by his investigation, the greater part of thearithmetic is found with sixteen sutras, or word-formula [7] [8]. These formulae por-
tray the ways in which mind sensibly works and are in this manner a remarkable assis-
tance in directing the pupil to the correct tactics for results. In [9] the Vedic scheme,
challenging complications or huge sums can regularly be solved instantly by this method.

Anurupye Algorithm

Anurupye Sutra accomplishes compliment by subtracting off a two numbers from its closest power index, i.e. 10, 20, 30, etc. Hence
size, of the multipliers with size 8-bit each is reduced by finding the difference of the
reference number from the nearest index. The Anurupye methods for multiplying de-
cimal numbers 32 × 36 are explained [7] with effective, simplified steps to produce bothLHS and RHS of the result

In this approach, we design a FIR filter by implementing a proposed Anurupyemultip-
lier algorithm. The conventional direct form structure with 8-Tap FIR filter is shown in

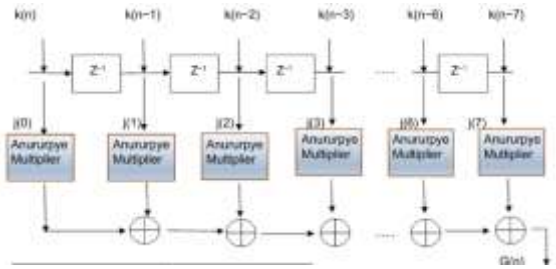


fig proposed multiplier

the Figure 2 use 8 numbers of multipliers, 7 numbers of additions for a single sample.

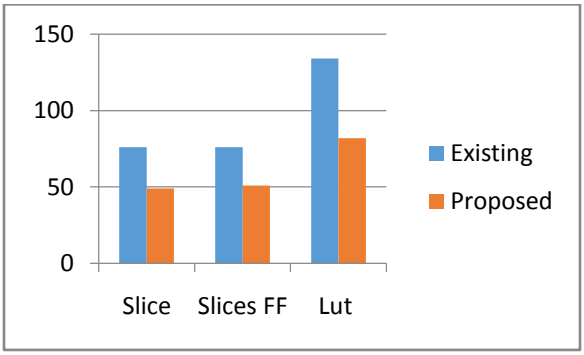
The conventional FIR design uses delay elements, which adds delay to the signal by
certain value by multiplying the values of the previous steps with the corresponding
coefficient. The same filter can be reduced by using Anurupye multiplier for calculating
product between inputs with the coefficient by replacing normal multiplication

RESULT

FIR filter design methods by utilizing modified minimum switching activity booth multiplier is examined in this paper. Fig shows design summary and performance analysis of our proposed system

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	76	960	7%
Number of Slice Flip Flops	76	1920	3%
Number of 4 input LUTs	134	1920	6%
Number of bonded IOBs	23	83	27%
Number of GCLKs	1	24	4%

s.no	Parameter	Existing	Proposed
1	Slice	76	49
2	Slices FF	76	51
3	Lut	134	82



CONCLUSION

In this paper, we have bestowed a unique approach to improve the performance of theFIR Filter considerably by using an Anurupye Vedic Multiplier. This proposed multiplier provides improved performance parameters with less number of gates used for agiven 8 × 8 bit multiplier. Also, from the results achieved it can be obviously apparentthat the delay of this multiplier is relatively reduced compared to the other commondesigns of multipliers. It's therefore, decided that the Anurupye Vedic Multiplier basedFIR filter design would be a good choice for high-speed DSP applications in the future.Further research can be performed with the other algorithms of Vedic mathematics andto obtain efficient design to be utilized in cryptography network for providing securedata transfer.

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